SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based upon and claims the benefit of priority of the prior Japanese Patent Application No. 2010-160115 filed on Jul. 14, 2010, the entire contents of which are incorporated herein by reference.

BACKGROUND

[0002] (i) Technical Field

[0003] A certain aspect of the embodiments discussed herein is related to a semiconductor device. Another aspect of the embodiments is related to a semiconductor device with an electrode shaped into steps.

[0004] (ii) Related Art

[0005] An FET (Field Effect Transistor) may be used as a semiconductor device that amplifies RF signals such as microwaves. The FET is configured to form a source electrode, a drain electrode and a gate electrode on a semiconductor substrate. Japanese Patent Application Publication. No. 2002-359257 discloses a multi-finger type FET in which source electrodes, drain electrodes and gate electrodes are arranged in the form of a tooth comb.

[0006] The magnitude of current that flows through an electrode of the semiconductor device is restricted by the tolerable current density, which depends on the material of the electrode. The restricted magnitude of current may not produce high power.

SUMMARY

[0007] According to an aspect of the present invention, there is provided A semiconductor device including: source electrodes that are provided on a semiconductor substrate and are having source fingers, the source fingers having stepwise side portions so that a length of the source fingers in a gate length direction decreases stepwise in a direction from ends of the source fingers connected to source pads towards other ends; drain electrodes that are provided on the semiconductor substrate and are having drain fingers, the drain fingers having stepwise side portions so that a length of the drain fingers in the gate length direction decreases stepwise in a direction from ends of the drain fingers connected to drain pads towards other ends, the stepwise side portions of the drain fingers corresponding to those of the source fingers; and gate electrodes that are provided, on the semiconductor substrate and have bent portions between steps formed in the stepwise side portions of the source fingers and steps formed in the stepwise side portions of the drain fingers, the gate electrodes being bent in the bent portions along the source fingers and the drain fingers, a shape of the stepwise side portion of one of the source fingers and that or the stepwise portion of a corresponding one of the drain fingers being symmetrical about a midpoint of an imaginary line that connects the other end of the one of the source fingers and the other end of the corresponding one of the drain fingers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. **1** is a plan view of a semiconductor device in accordance with a first embodiment;

[0009] FIG. **2**A illustrates a source electrode and a drain electrode used in the semiconductor device in FIG. **1**, and FIG. **2**B is an enlarged view of a bent portion and its vicinity in the semiconductor device illustrated in FIG. **1**;

[0010] FIG. **3** is a graph that illustrates a relationship between the number of steps and a gate pitch;

[0011] FIGS. **4**A through **4**C are respectively cross-sectional views of a bent portion and its vicinity;

[0012] FIG. **5**A is a plan view of a semiconductor device, in accordance with a second embodiment, and FIG. **5**B is an enlarged view of a bent portion and its vicinity in the semiconductor device illustrated in FIG. **5**A;

[0013] FIGS. **6**A and **6**B are respectively cross-sectional views of the semiconductor device in accordance with the second embodiment;

[0014] FIG. **7** is a graph of a relationship between the gain and the unit gate width;

[0015] FIG. **8**A is a plan view of a semiconductor device in accordance with a third embodiment, and FIG. **8**B is a cross-sectional view taken along a line D-D in FIG. **8**A;

[0016] FIG. **9** is a plan view of a semiconductor device in accordance with a fourth embodiment;

[0017] FIG. **10** is a plan view of a semiconductor device in accordance with a fifth embodiment; and

[0018] FIG. **11** is a plan view of a semiconductor device in accordance with a sixth embodiment.

DETAILED DESCRIPTION

[0019] A description is now given of embodiments of the present invention with reference to the drawings.

First Embodiment

[0020] FIG. **1** is a plan view of a semiconductor device in accordance with a first embodiment. FIG. **2**A is a view of a source electrode and a drain electrode, and FIG. **2**B is an enlarged view of a bent portion and its vicinity in FIG. **2**A. An X direction in FIG. **1** is a gate length direction, and a Y direction is a gate width direction. FIG. **2**A illustrates a pair of source electrode **12** and drain electrode **14** extracted from FIG. **1**. FIG. **2**B has an enlarged view of a portion surrounded by a dashed-line ellipse.

[0021] As illustrated in FIG. **1**, a semiconductor device **100** of the first embodiment includes a semiconductor substrate **10**, source electrodes **12**, drain electrodes **14** and gate electrodes **16**. The semiconductor substrate **10** may have a nitride semiconductor layer. As will be described later, the semiconductor substrate **10** may be formed by stacking a GaN (gallium nitride) layer on a substrate made of SiC (silicon carbide), for example, and stacking an n-type AlGaN (aluminum gallium nitride) on the GaN layer. The GaN layer functions as a channel layer. The n-AlGaN layer functions as an electron supply layer. Active regions and inactive regions are formed in the upper surface of the semiconductor substrate **10**. In the active regions, the carriers move and current flows between the drain and source. In the inactive regions, the carrier do not move and current does not flow between the drain and source. The inactive regions may be formed by removing the channel layer or by making the channel layer inactive by ion implantation. In the semiconductor substrate **10**, in the Y direction, there are formed, from the lower side of FIG. **1**, an inactive region **20**, an active region **21**, an inactive region **22**, an active region **23**, an inactive region **24**, an active region **25** and an inactive region **26**. In FIG. **1**, the active regions **21**, **23** and **25** are illustrated with diagonal grids. The active regions **21**, **23** and **25** have an identical width.